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(54) **BACK SIDE ILLUMINATION IMAGE SENSOR AND MANUFACTURING METHOD THEREOF**

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H01L 27/146	(2006.01)

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CPC ***H01L 27/14621*** (2013.01); ***H01L 27/1464*** (2013.01); ***H01L 27/14687*** (2013.01)

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See application file for complete search history.

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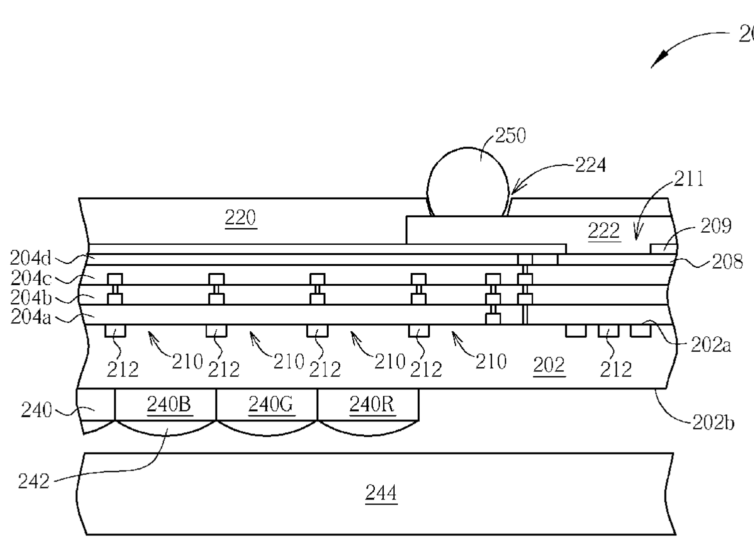
(57) **ABSTRACT**

A manufacturing method of a BSI image sensor includes providing a substrate having a plurality of photo-sensing elements and a plurality of multilevel interconnects formed on a first side of the substrate; forming a redistribution layer (RDL) and a first insulating layer covering the RDL on the front side of the substrate; providing a carrier wafer formed on the front side of the substrate; forming a color filter array (CFA) on a second side of the substrate, the second side being opposite to the first side; removing the carrier wafer; and forming a first opening in the first insulating layer for exposing the RDL.

8 Claims, 8 Drawing Sheets



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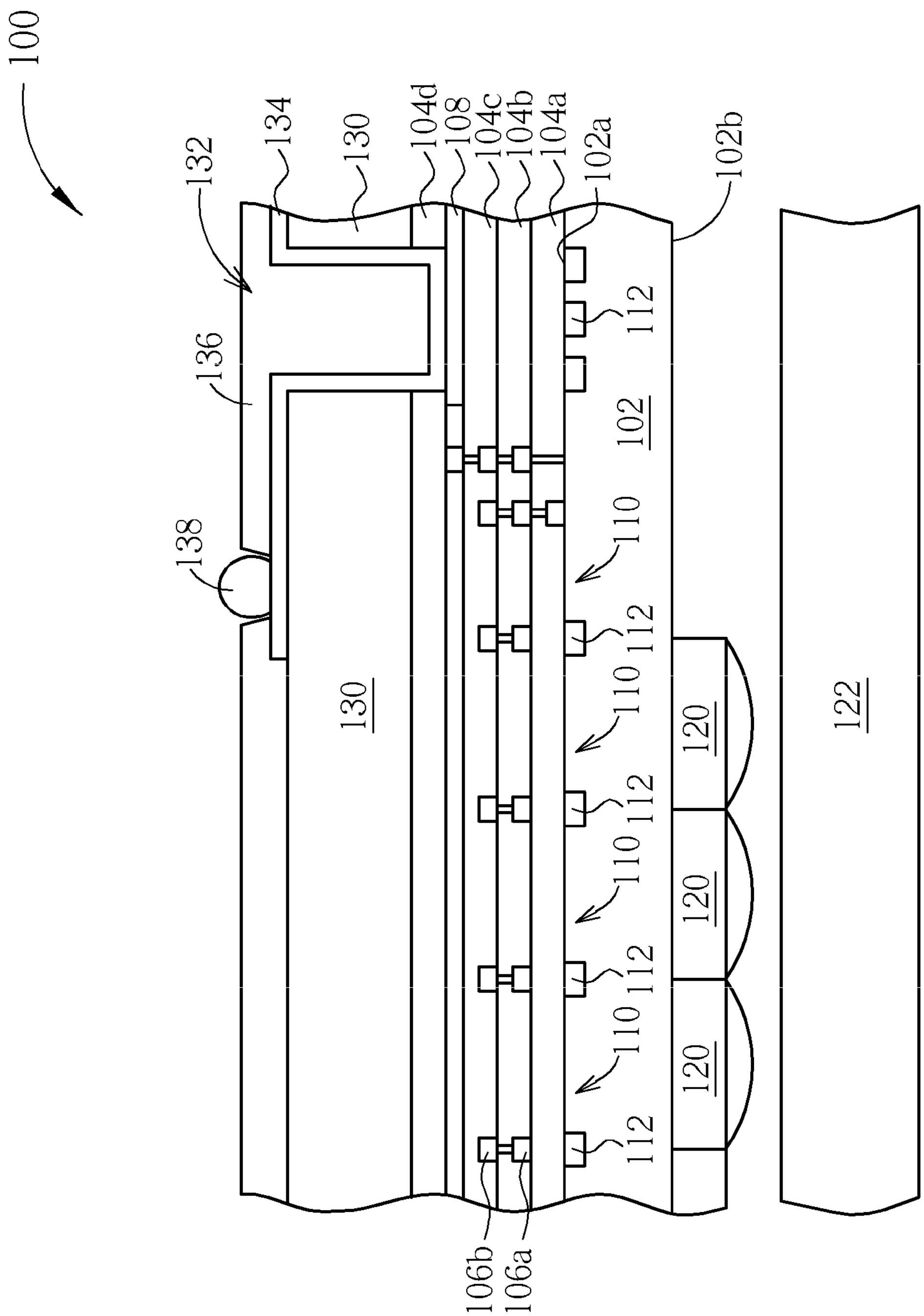
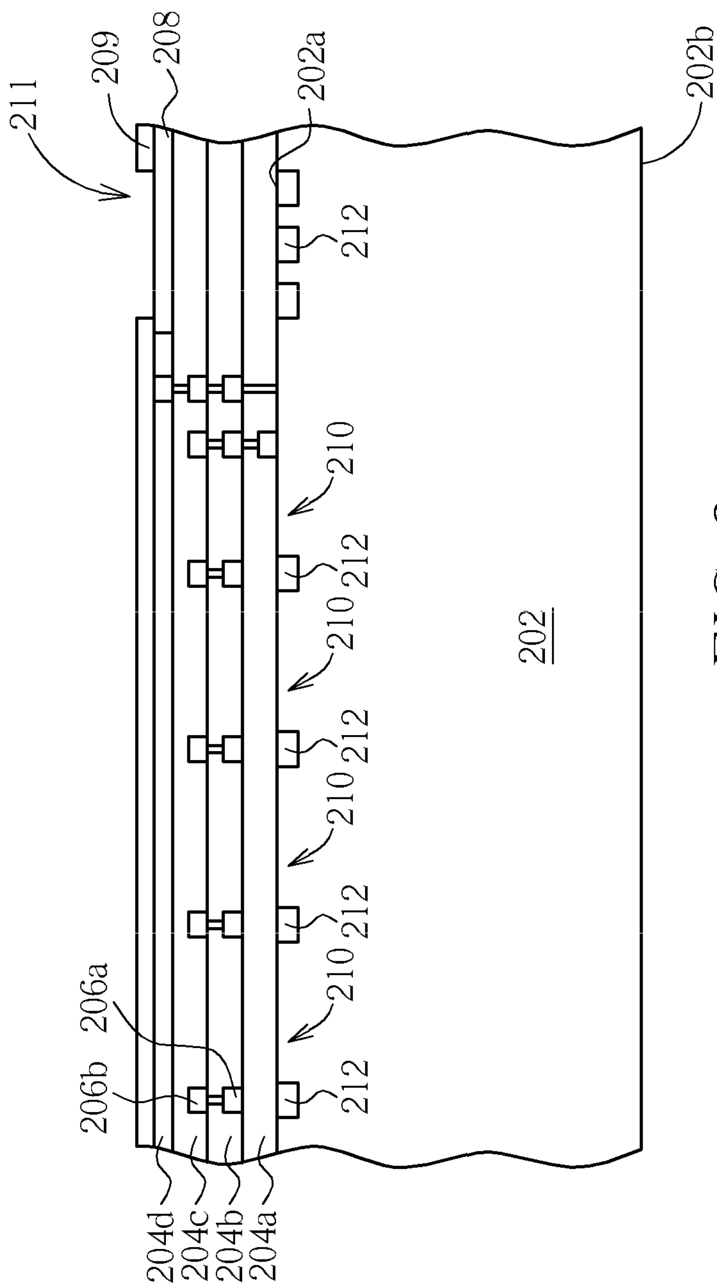


FIG. 1 PRIOR ART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202a
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212
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202
206a
206b
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204c
204b
204a

FIG. 2

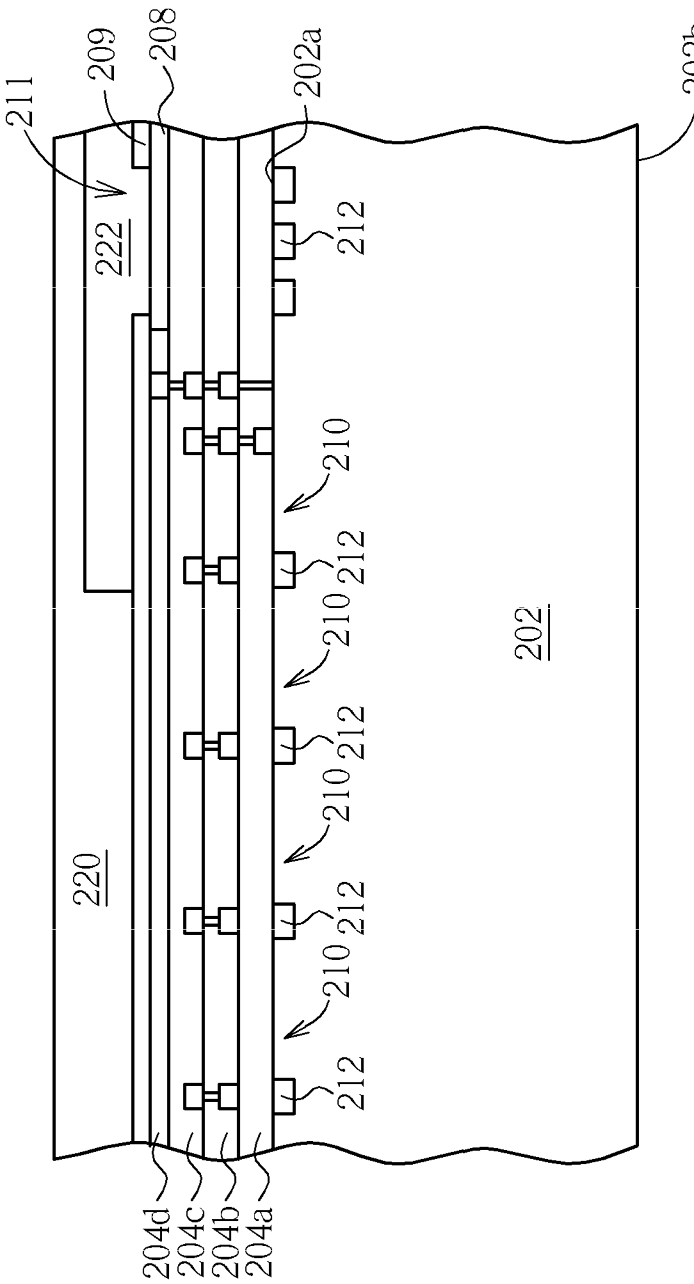
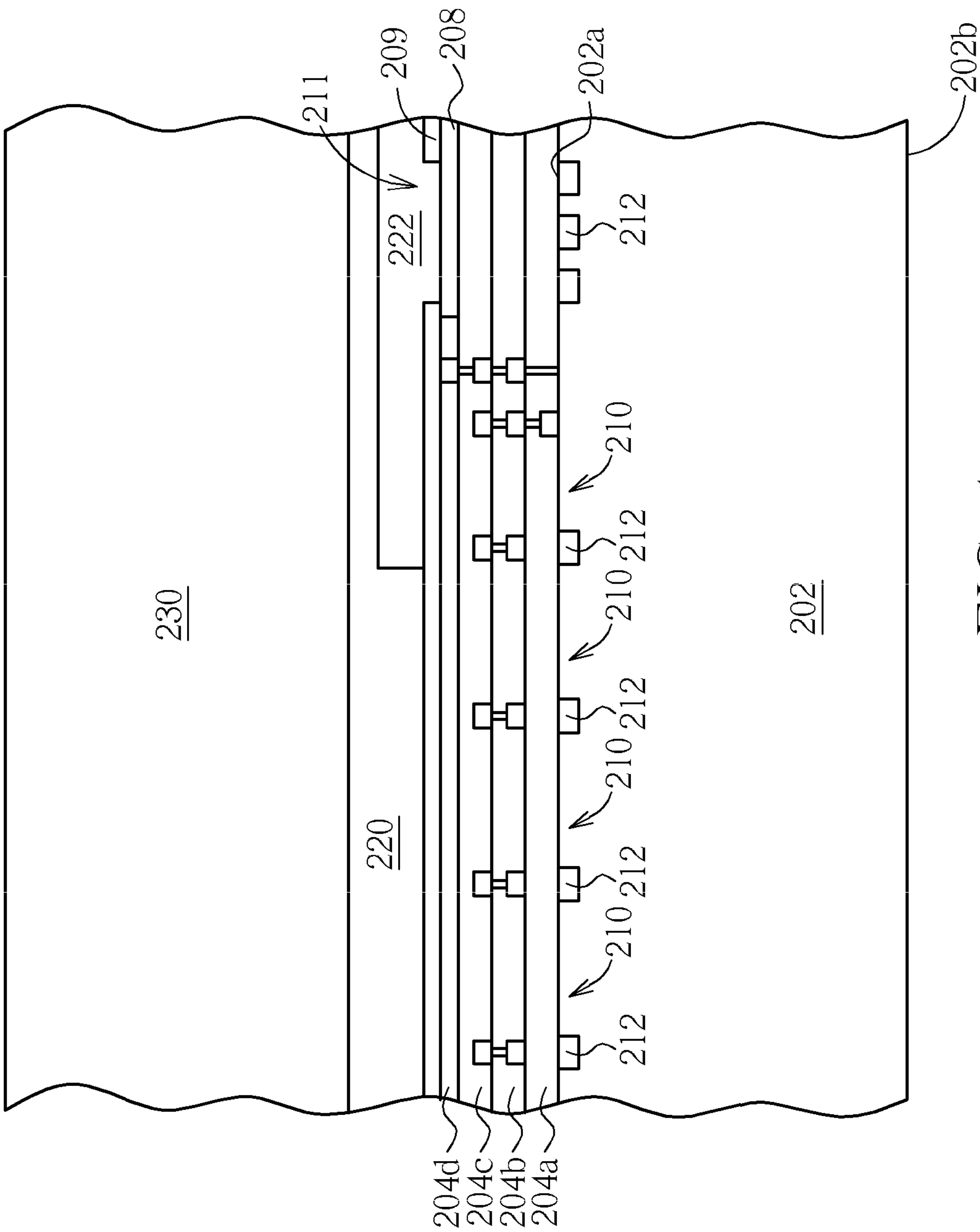


FIG. 3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209
208
202a
202b
222
212
210
212
210
212
210
212
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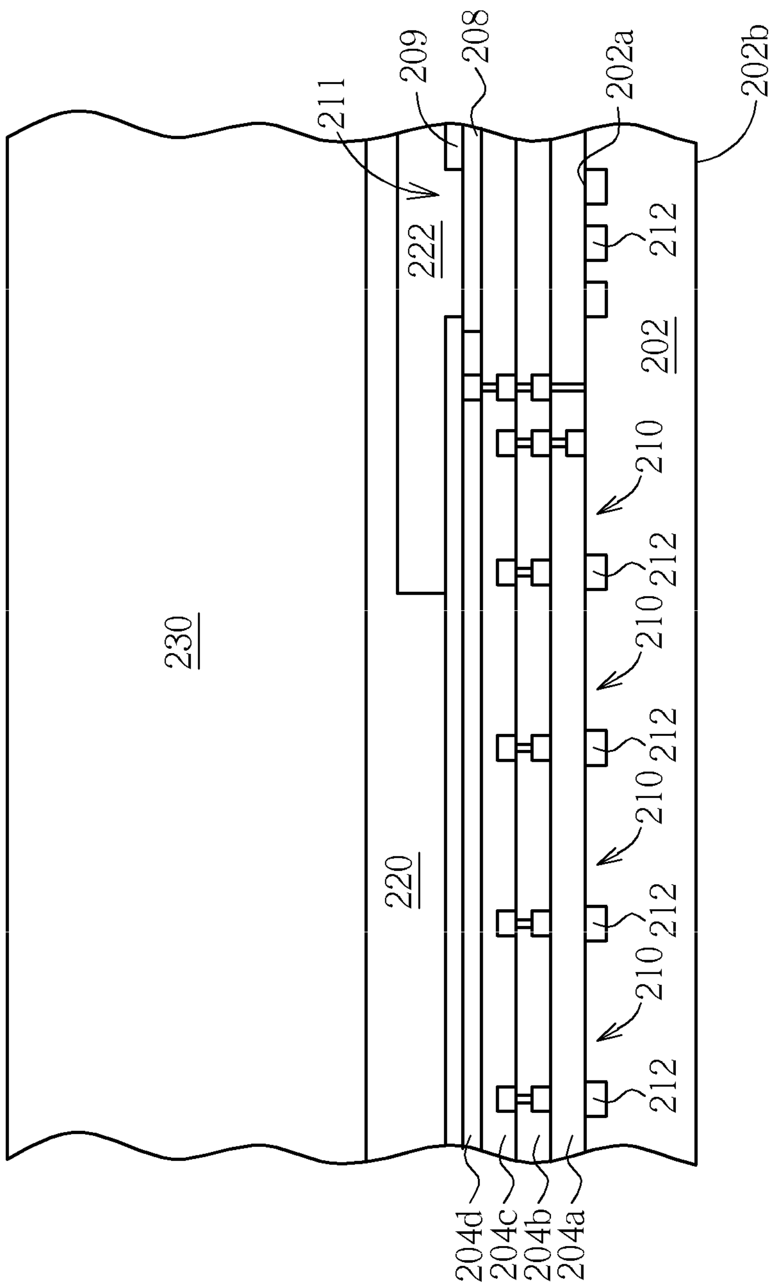
212
230
220
202
204d
204c
204b
204a

FIG. 4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208
202a
202b
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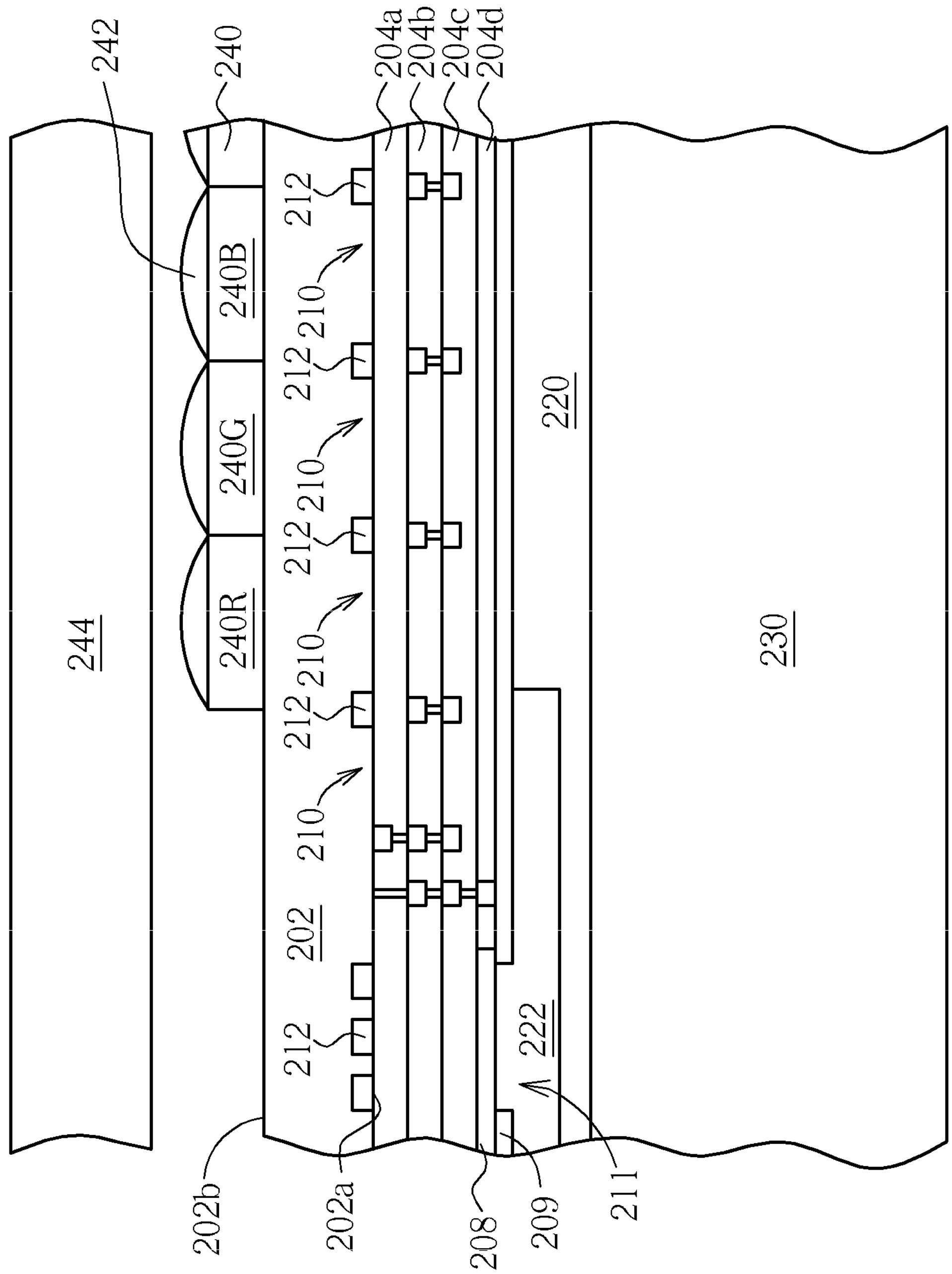
212
202
210
230
220
204d
204c
204b
204a

FIG. 5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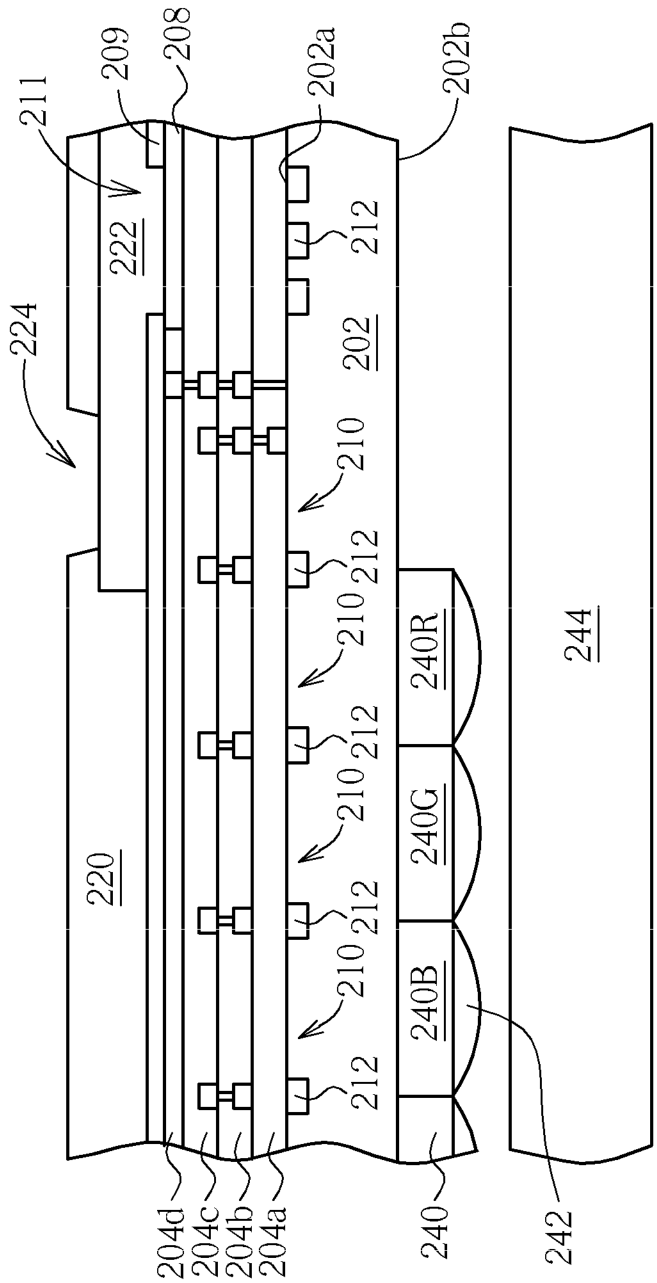
204b
204c
204d
240B
240G
240R
244
212
210
220
230
202
222
202b
202a
208
209
211

FIG. 6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202a
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222
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224
202
210
212
210
240R
244
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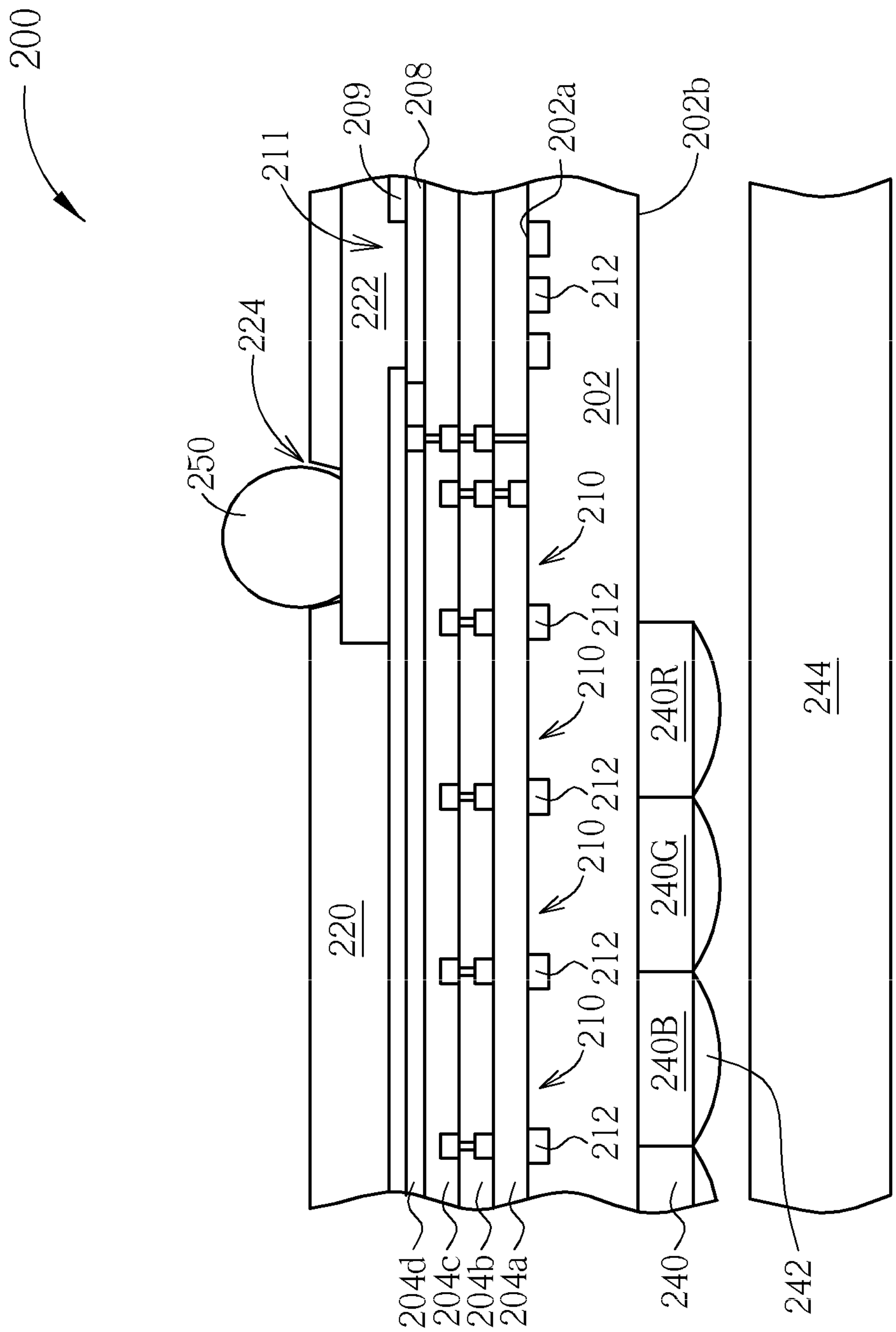
210
240G
220
212
210
240B
212
204d
204c
204b
204a
240
242

FIG. 7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211
209
208
202a
202b
222
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202
250
210
212
210
240R
244
212
210
240G
220
212
210
240B
212
204d
204c
204b
204a
240
242

FIG. 8

BACK SIDE ILLUMINATION IMAGE SENSOR AND MANUFACTURING METHOD THEREOF

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to an image sensor and a manufacturing method thereof, and more particularly, to a back side illumination (BSI) complementary metal oxide semiconductor (CMOS) image sensor and manufacturing method thereof.

2. Description of the Prior Art

CMOS image sensors (hereinafter abbreviated as CIS) are widely used in various applications such as digital camera. The CIS are used for sensing a volume of exposed light projected towards a semiconductor substrate. To do this, the CIS use an array of pixels, or image sensor elements, to collect photo energy to convert images into electrical signals that can be used in a suitable application. A CIS pixel includes a photodetector such as a photodiode, photogate detector, or phototransistor, to collect photo energy.

One form of CIS, backside-illuminated (BSI) CIS, sense a volume of light projected towards the back side surface of the substrate of the sensor by using pixels located on the front side of the substrate. Please refer to FIG. **1**, which is a schematic drawing illustrating a conventional BSI CIS **100**. As shown in FIG. **1**, the conventional BSI CIS **100** includes a thinned silicon substrate **102** having a plurality of photodiode regions **110**. The photodiode regions **110** are electrically isolated from each other by a plurality of shallow trench isolations (STIs) **112**. The conventional BSI CIS **100** also includes a plurality of dielectric layers **104***a*, **104***b*, **104***c* and **104***d*, by which a plurality of metal layers **106***a*, **106***b* are respectively sandwiched therebetween, formed on the silicon substrate **102**. Said dielectric layers and the metal layers construct the multilevel interconnects as shown in FIG. **1**. For simplifying the features of the conventional BSI CIS **100**, all the transistor devices are omitted. The conventional BSI CIS **100** is photosensitive to light incident upon the back side **102***b* of the silicon substrate **102**, therefore the conventional BSI CIS **100** further includes a color filter array (CFA) **120** respectively corresponding to the photodiode regions **110** formed on the back side **102***b* of the silicon substrate **102**. And a glass **122** is subsequently formed on the back side **102***b* of the silicon substrate **102**.

The BSI CIS **100** is advantageous in that they provide higher fill factor and reduced destructive interference. However, the silicon substrate **102** must be thin enough that light projected towards the back side **102***b* of the silicon substrate **102** can reach the pixels. Therefore, a silicon carrier wafer **130** is always in need to provide support for the thinned silicon substrate **102**. As shown in FIG. **1**, the silicon carrier wafer **130** is bonded to the front side **102***a* of the silicon substrate **102** before forming the CFA **120**. For providing output electrical connection for the BSI CIS **100**, a through-silicon via (TSV) **132** is formed to penetrate the silicon carrier wafer **130** and thus expose a bonding pad **108** after forming the CFA **120**. Then, a redistribution layer **134**, a passivation layer **136**, and a solder ball **138** are formed as shown FIG. **1**. Additionally, the silicon carrier wafer **130** is sandwiched between the insulating layer **104***d* and the passivation layer **136** as shown in FIG. **1**.

It is noteworthy that the conventional BSI CIS **100** always faces a requirement of low thermal budget due to the CFA **120** formed on the back side **102***b* of the silicon substrate **100**. In detail, while the CFA **120** lowers the thermal budget to 200° C.-250° C., the temperatures for forming the passivation layer **130**, the RDL **134**, and the solder ball **138** are all higher than 250° C. It is found that the CFA **120** suffers damages after forming the above mentioned elements. Furthermore, the TSV technique, which forms to penetrate the silicon carrier wafer **130**, also complicates the process.

Briefly speaking, though the BSI CIS **100** has the advantages of higher fill factor and reduced destructive interference, it still has more problems in process integration and process control. As such, an improved BSI CIS and manufacturing method thereof is desired.

SUMMARY OF THE INVENTION

According to an aspect of the present invention, a manufacturing method of a BSI image sensor is provided. The manufacturing method includes providing a substrate having a plurality of photo-sensing elements and a plurality of multilevel interconnects formed on a first side of the substrate; forming a redistribution layer (RDL) and a first insulating layer covering the RDL on the first side of the substrate; providing a carrier wafer formed on the first side of the substrate; forming a color filter array (CFA) on a second side of the substrate, the second side being opposite to the first side; removing the carrier wafer; and forming a first opening in the first insulating layer for exposing the RDL.

According to another aspect of the present invention, a BSI image sensor is provided. The BSI image sensor includes a substrate having a front side and a back side, a first insulating layer formed on the front side of the substrate, a second insulating layer formed directly on the first insulating layer, a first opening formed in the first insulating layer, and a redistribution layer (RDL) formed in the first opening. Furthermore, sidewalls of the first opening are surrounded by the first insulating layer.

According to the present invention, elements formed at process temperatures higher than the thermal budget of the CFA are all fabricated before forming the CFA, therefore those temperatures render no impact to the CFA. Consequently, the CFA of the BSI image sensor provided by the present invention never suffers damages from high temperatures. Secondly, since the carrier wafer is removed from the substrate, no TSV technique is required, therefore the process is simplified.

These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic drawing illustrating a conventional BSI CIS.

FIGS. **2**-**8** are schematic drawings illustrating a manufacturing method for a BSI image sensor provided by a preferred embodiment of the present invention, wherein

FIG. **3** is a schematic drawing in a step subsequent to FIG. **2**,

FIG. **4** is a schematic drawing in a step subsequent to FIG. **3**,

FIG. **5** is a schematic drawing in a step subsequent to FIG. **4**,

FIG. **6** is a schematic drawing in a step subsequent to FIG. **5**,

FIG. 7 is a schematic drawing in a step subsequent to FIG. 6, and

FIG. 8 is a schematic drawing in a step subsequent to FIG. 7.

DETAILED DESCRIPTION

Please refer to FIGS. 2-8, which are schematic drawings illustrating a manufacturing method for a BSI image sensor provided by a preferred embodiment of the present invention. As shown in FIG. 2, the preferred embodiment first provides a substrate **202**. The substrate **202** has a first side **202***a* and a second side **202***b* opposite to the first side **202***a*. For example, the first side **202***a* is the front side of the substrate **202** and the second side **202***b* is the back side of the substrate **202**. The substrate **202** includes a plurality of photo-sensing elements **210**, such as photodiode regions, which are electrically isolated from each other by shallow trench isolations (STIs) **212**. A plurality of dielectric layers **204***a*, **204***b*, **204***c* and **204***d*, by which a plurality of metal layers **206***a*, **206***b* are respectively sandwiched therebetween, is formed on the substrate **202**. Said dielectric layers and the metal layers construct a plurality of multilevel interconnects. A bonding pad **208** is formed on the topmost dielectric layer **204***d* and covered by an insulating layer **209**. Please note that all the transistor devices of the BSI image sensor are omitted, but those skilled in the art should not ignore those elements. Furthermore, the photo-sensing elements **210** and the multilevel interconnects are all formed in the front side **202***a* of the substrate **202**.

Please still refer to FIG. 2. Then an opening **211** is formed in the insulating layer **209** and the opening **211** exposes a portion of the bonding pad **208**. It is noteworthy that sidewalls of the opening **211** are only surrounded by the insulating layer **209**.

Please refer to FIG. 3. After forming the opening **211**, a redistribution layer (RDL) **222** is formed on the front side **202***a* of the substrate **202** and followed by forming another insulating layer **220**, such as a passivation layer directly on the insulating layer **209** and the RDL **222**. As shown in FIG. 3, the RDL **222** is formed in the opening **211** and electrically connected to the bonding pad **208** through the opening **211**. The RDL **222** and the insulating layer **220** are formed at temperatures higher than 250° C. It is noteworthy that the insulating layer **220** is formed to cover the RDL **222** entirely. Therefore, a thickness of the insulating layer **220** is larger than a thickness of the RDL **222**. The insulating layer **220** having the desired thickness can be formed by conventional film formation methods. And a planarization process can be performed to thin down the insulating layer **220** if required.

Please refer to FIG. 4. Subsequently, a carrier wafer **230** is provided and formed on the front side **202***a* of the substrate **202**. Specifically speaking, the carrier wafer **230** is formed on the insulating layer **220**. The carrier wafer **230** is bonded to the insulating layer **220** by commonly used bonding materials (not shown), such as a photoresist, epoxy, or UV tape, but is not limited to those materials.

Please refer to FIG. 5. After bonding the carrier wafer **230** to the substrate **202**, a wafer thinning process is performing to the substrate **202**. The wafer thinning process includes a grinding process, a polishing process, a plasma etching process, a wet etching process, or any combinations of the above processes. Because the substrate **202** must be thin enough that light projected towards the back side **202***b* of the substrate **202** can reach the photo-sensing elements **210** formed in the front side **202***a*, the substrate **202** is thinned from the back side **202***b*. Accordingly, the substrate **202** includes a reduced thickness after the wafer thinning process, and the reduced thickness is between 1.8 micrometer (μm) and 3 μm. It is well-known that the thinned substrate **202** is very fragile; therefore the carrier wafer **230** provides support to the thinned substrate **202**.

Please refer to FIG. 6. After the wafer thinning process, the substrate **202** is flipped and a color filter array (CFA) **240** is formed on the back side (that is the second side) **202***b* of the substrate **202**. The CFA **240** includes a plurality of color filters **240**R/**240**G/**240**B, and as shown in FIG. 6, each color filer **240**R/**240**G/**240**B is formed respectively corresponding to a photodiode region **210**. Subsequently, microlens **242** respectively corresponding to the color filters **240**R/**240**G/**240**B are formed on the CFA **240**. Then, a transparent protecting member, for example but not limited to a glass substrate **244**, is formed on the back side **202***b* of the substrate as shown in FIG. 6.

Please refer to FIG. 7. Next, the substrate **202** is flipped back and followed by removing the carrier wafer **230** from the front side (that is the first side) **202***a*. After removing the carrier wafer **230**, an opening **224** is formed in the insulating layer **220**. It should be noted that the opening **224** is formed to expose the RDL **222**. More important, the opening **224** and the opening **211** are spaced apart from each other.

Please refer to FIG. 8. After forming the opening **224**, a conductive structure **250**, such as a solder ball, electrically connected to the RDL **222** is formed in the opening **224**. Consequently, a BSI image sensor **200** is obtained.

According to the present invention, elements formed at process temperatures higher than the thermal budget of the CFA are all fabricated before forming the CFA, therefore those temperatures render no impact to the CFA. Consequently, the CFA of the BSI image sensor provided by the present invention never suffers damages from high temperatures. Secondly, since the carrier wafer is removed from the substrate, no TSV technique is required, therefore the process is simplified.

Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

What is claimed is:

1. A manufacturing method of a back side illumination (BSI) image sensor, comprising:

providing a substrate having a plurality of photo-sensing elements and a plurality of multilevel interconnects formed on a first side of the substrate;

forming a bonding pad and a first insulating layer covering the bonding pad on the first side of the substrate;

forming a redistribution layer (RDL) and a second insulating layer covering the RDL on the first insulating layer, the RDL being electrically connected to the bonding pad;

providing a carrier wafer formed on the first side of the substrate after forming the RDL and the second insulating layer;

performing a wafer thinning process to a second side of the substrate after providing the carrier wafer, the second side being opposite to the first side;

forming a color filter array (CFA) on the second side of the substrate after performing the wafer thinning process;

removing the carrier wafer; and

forming a second opening in the second insulating layer on the first side of the substrate for exposing the RDL after removing the carrier wafer.

2. The manufacturing method of a BSI image sensor according to claim 1, further comprising forming a first opening in the first insulating layer for exposing the bonding pad before forming the RDL.

3. The manufacturing method of a BSI image sensor according to claim 2, wherein the RDL electrically connected to the bonding pad through the first opening.

4. The manufacturing method of a BSI image sensor according to claim 2, wherein the first opening and the second opening are spaced apart from each other.

5. The manufacturing method of a BSI image sensor according to claim 1, further comprising performing a planarization process to the second insulating layer before providing the carrier wafer.

6. The manufacturing method of a BSI image sensor according to claim 1, wherein the substrate comprises a reduced thickness after the step of thinning the substrate, and the reduced thickness is between 1.8 micrometer (μm) and 3 μm.

7. The manufacturing method of a BSI image sensor according to claim 1, further comprising forming a protecting member on the CFA.

8. The manufacturing method of a BSI image sensor according to claim 1, further comprising forming a conductive structure electrically connected to the RDL in the second opening.

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